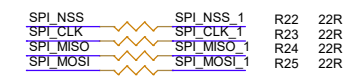
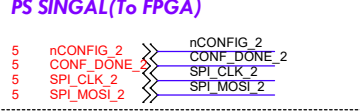
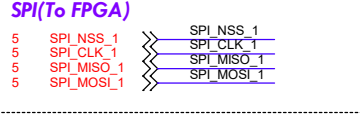
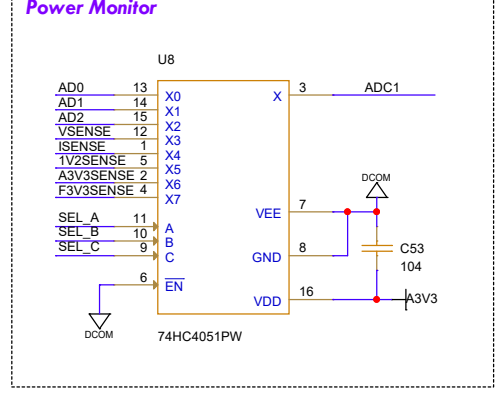
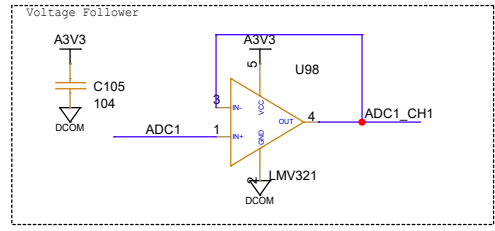
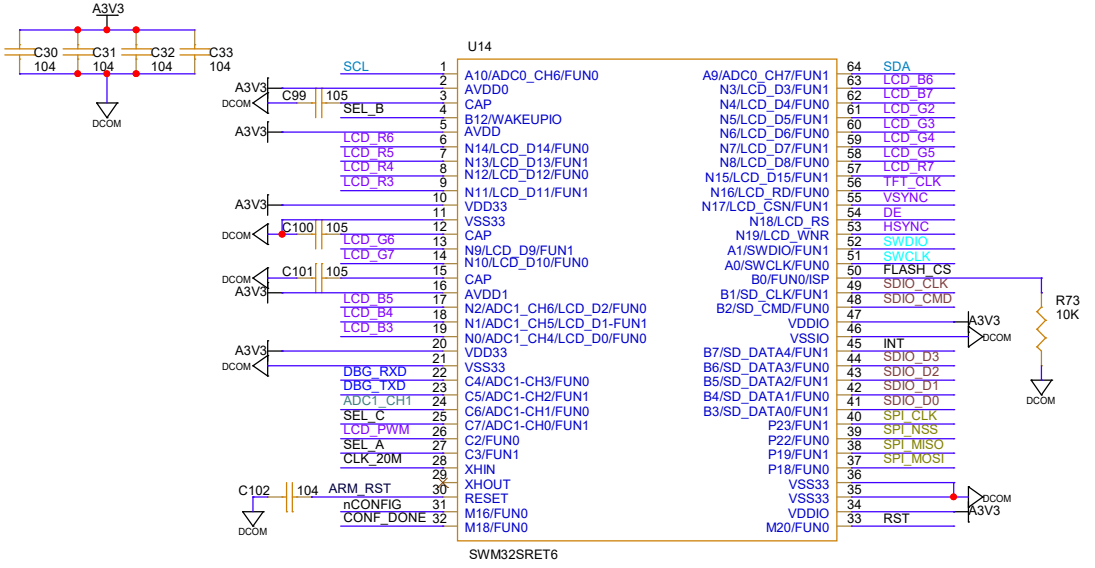
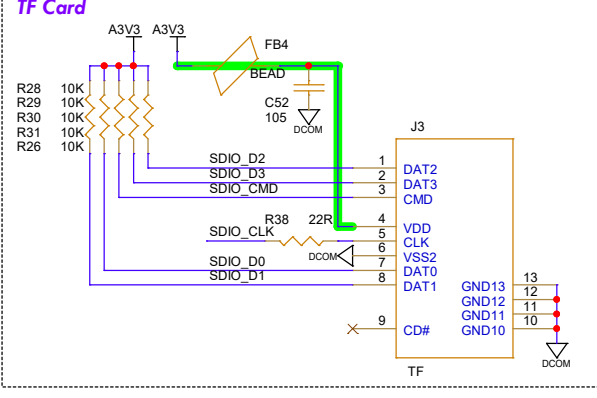
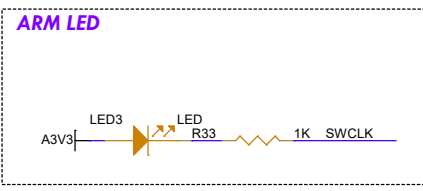
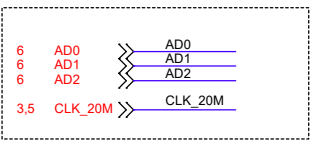
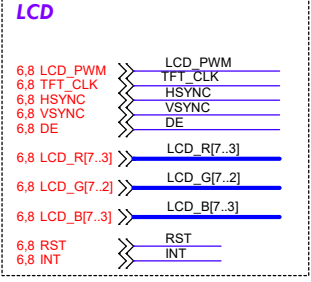
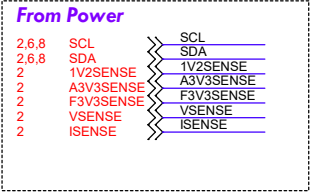
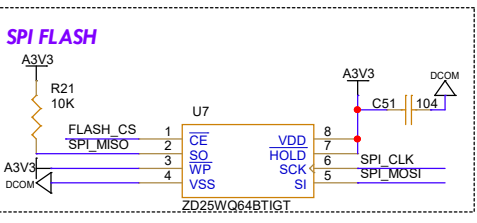
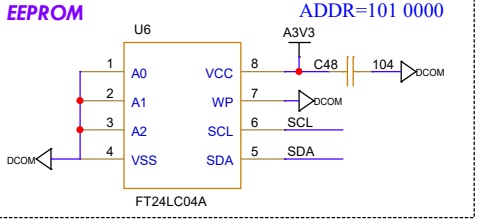
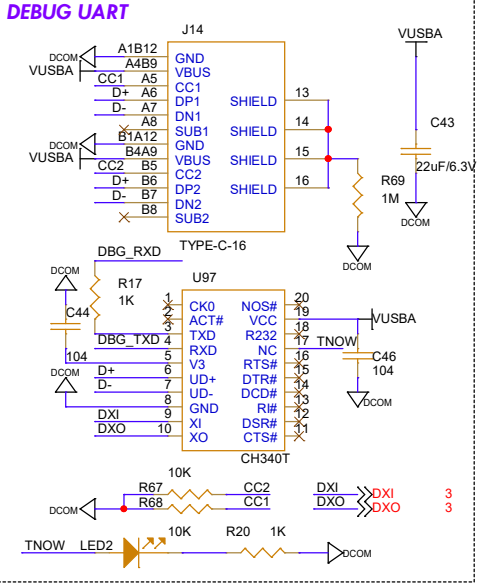
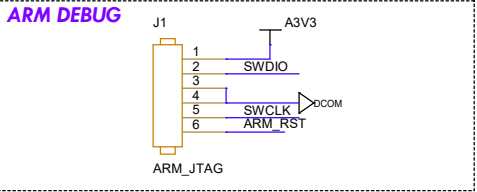
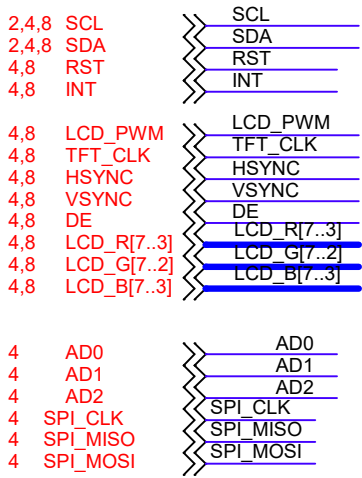


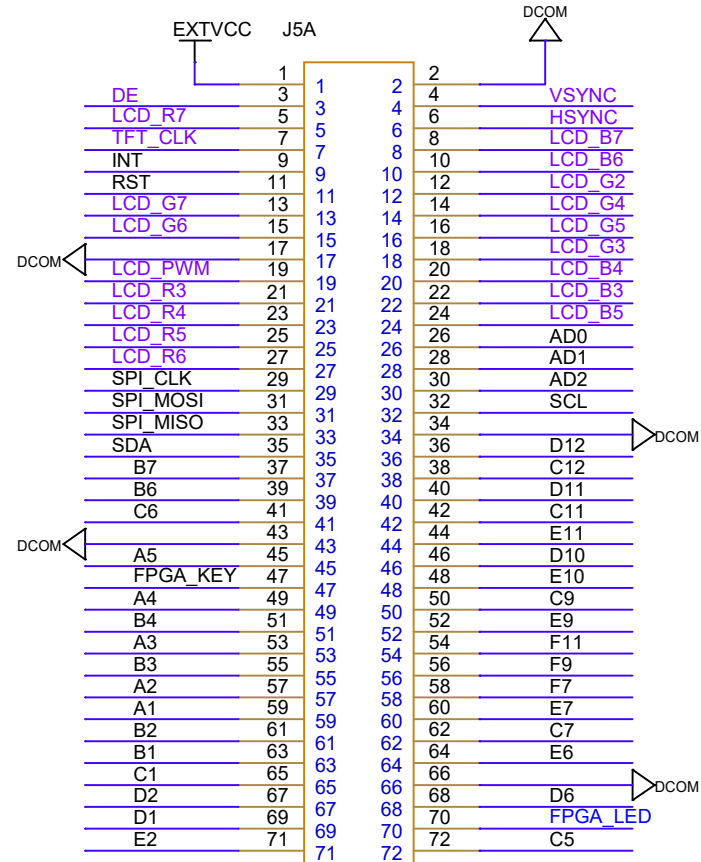
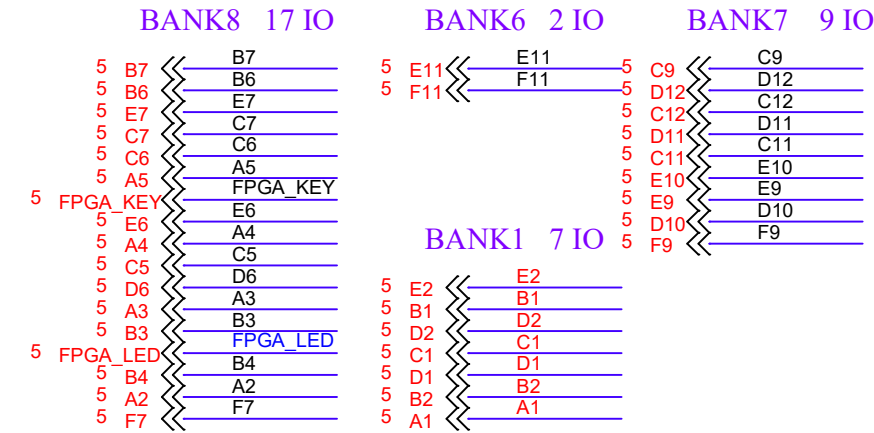
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ARM IO 31



FPGA IO 35



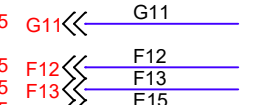
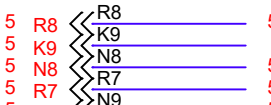
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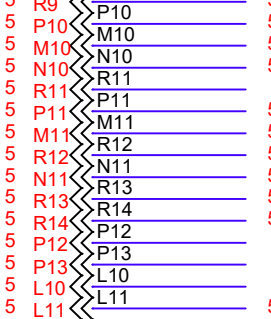
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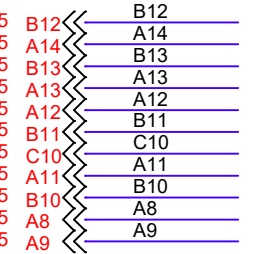
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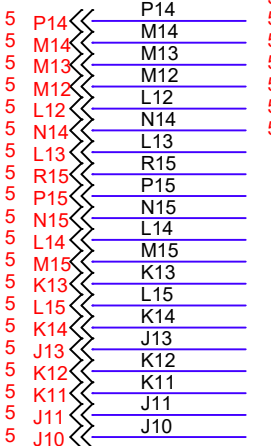
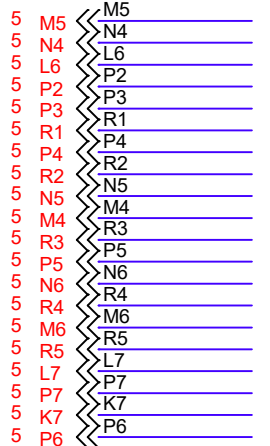


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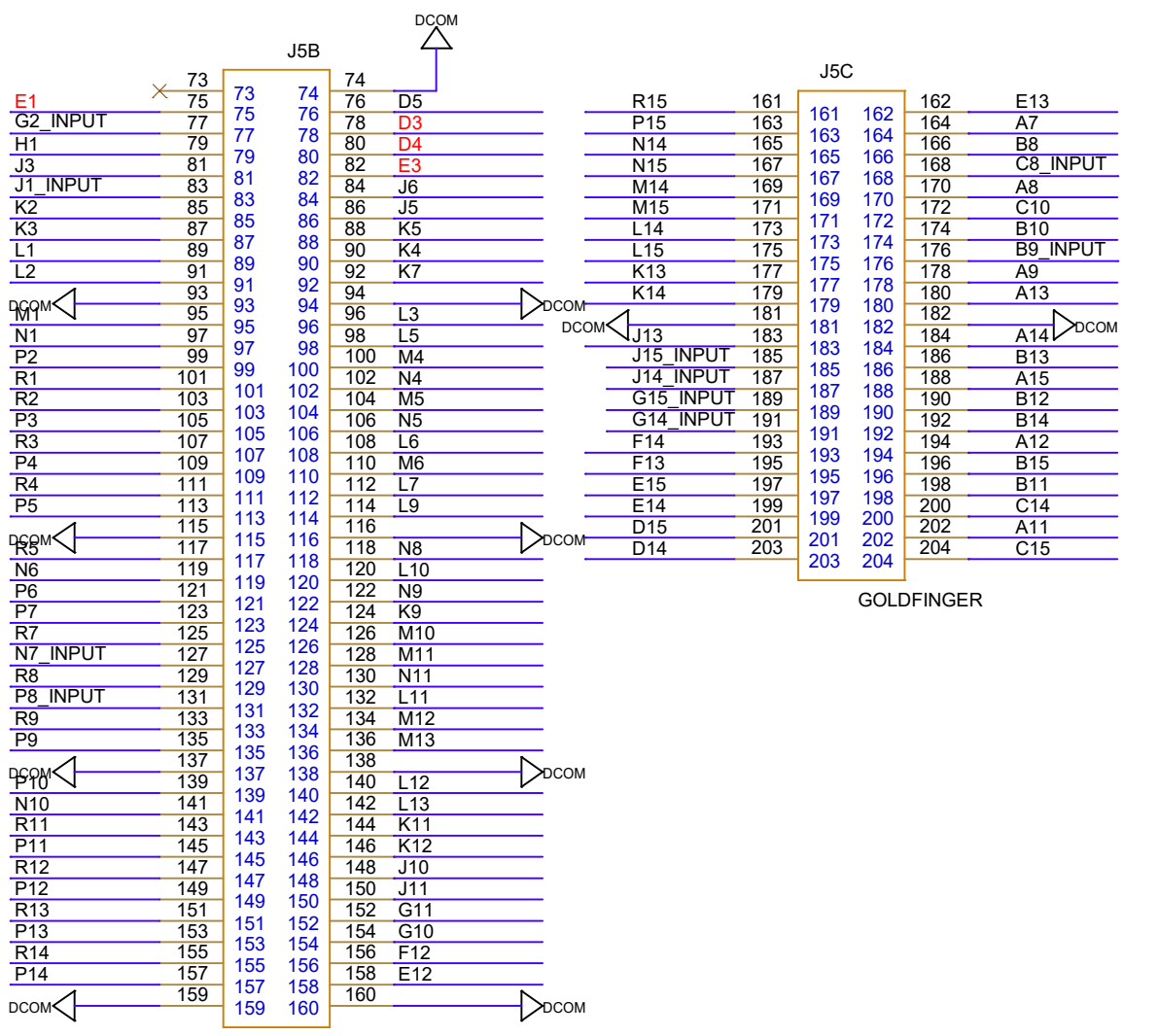
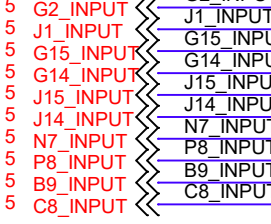
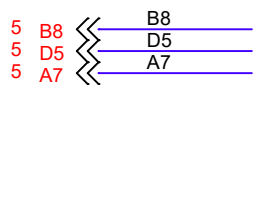
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BANK5 20 IO



BANK8 3 IO

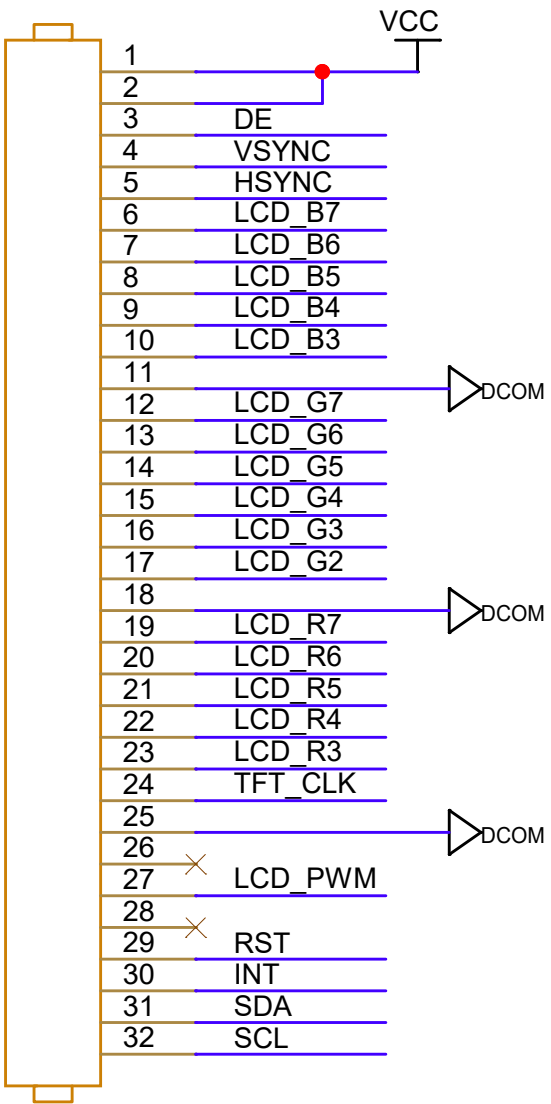
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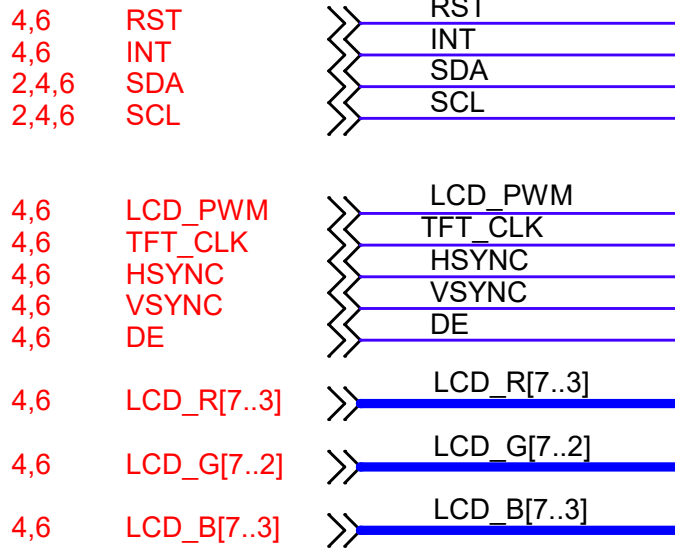
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